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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,769	05/14/2001	Takashi Hotta	500.28166CX2	7218

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EXAMINER

PAN, DANIEL H

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/853,769

Applicant(s)

HOTTA ET AL.

Examiner

Daniel Pan

Art Unit

2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 May 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 13-15 is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☒ Claim(s) 3-11 and 12 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 May 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☒ Certified copies of the priority documents have been received in Application No. 07/433,368.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>05/14/01</u> . | 6) <input type="checkbox"/> Other: _____ |

1. Clams 1-16 are presented for examination.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1,2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Horikawa (4,631,669) in view of Watsons et al (3,573,853)

3. As to claim 1, Horikawa disclosed a system including at least :

- a) a program counter col.5., lines 65-68, col.6, lines 1-9);
- b) m instruction registers (see instruction register [32] in col.3, lines 20-23, see also the instruction register 70 in line 33);
- b) register file [register file 30] for storing data (see the data stored in register file 30 in col.5, lines 21-24, see also RF 58 in fig.1);
- c) m arithmetic units [U1 ALU 36] [U2 ALU 66] for reading data from the register file and made arithmetic operations in parallel (see concurrent operations of the U1 and U2 in col.3, lines 3-8, col.5, lines 31-35).

4. As to the reading of instructions at one machine cycle, Horikawa also including the reading of instructions [A][B] at a given machine cycle (e.g. see fig.3, cycle 3).

Art Unit: 2183

5. Horikawa did not specifically show the content of his program counter was increased by m sequential address locations at a time as claimed. However, Watsons disclosed a system including a program counter which increased by m sequential address locations at a time (see the address register advanced by 8 at a time in col.12, lines 56—65). It would have been obvious to one of ordinary skill in the art to use Watsons in Horikawa for including the program counter for increasing the content by m sequential address locations as claimed because the use of Watsons could provide the processing capability of Horikawa to accept the instructions in groups which were sequentially fetched, thereby increasing the processing bandwidth of the plurality of instruction registers in Horikawa, and it could be readily achieved by defining the program counter of Watsons into Horikawa with modified configuration parameters, such as the fetch length of the instructions, recognizable by Horikawa, and because Horikawa also taught the bus contention by the separate processing units (e.g. see background in col.1, lines 31-61), which was an indication of the need for providing a greater bus width, and therefore, greater program counter range, such as a sequential block, in order to accept a greater number of instructions for enhancing the instructions bandwidth of the system, and Watsons did show the counter of increased by m (i.e. $m=8$), and for the above reasons, provided a motivation.

6. As to claim 2, Watsons's instruction was also fixed (see the instruction word of 32 bits in col.6, lines 29-46).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claim 16 is rejected under 35 U.S.C. 102(a)(b) as being anticipated by Horikawa (4,631,669).

8. As to claim 16, Horikawa disclosed a system including at least :

a) a program counter (col.5,, lines 65-68, col.6, lines 1-9);

b) m instruction registers (see, instruction registers in fig.1, see also the plural instruction registers [32] in col.3, lines 20-23, see also the instruction register 70 in line 33);

b) register file [register file 30] for storing data (see the data stored in register file 30 in col.5, lines 21-24, see also RF 58 in fig.1);

c) m arithmetic units [U1 ALU 36] [U2 ALU 66] for reading data from the register file and made arithmetic operations in parallel (see concurrent operations of the U1 and U2 in col.3, lines 3-8, col.5, lines 31-35).

9. As to the reading of instructions at one machine cycle, Horikawa also including the reading of instructions [A][B] at a given machine cycle (e.g. see fig.3, cycle 3).

Art Unit: 2183

10. Claims 3-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the combined features of the detection of the conflicting instruction and the execution only in one machine cycle.

11. Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record further teaches the condition flag and the means for detecting the presence of a conditional branch at a predetermined address to suppress the execution after the corresponding address of hem instructions at the satisfied condition.

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. None of the prior art of record teaches the instruction form part of the ROM.

12. Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the

Art Unit: 2183

base claim and any intervening claims. None of the prior art of record further recites the inhibition of interrupt between the m instructions which were read at a time.

13. Clams 13-15 are allowable over the art of record for showing only the content of the program counter within the limited range, the first address indicated in the instruction registers , and the out of range of the program counter read in the instruction registers and processed in parallel by z arithmetic operation u nits.

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a)Wilhite et al. (4,521,850) is cited for the basic teaching of the reading of instruction groups (e.g. see col.4, lines 7-33).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

Application/Control Number: 09/853,769

Page 7

Art Unit: 2183

For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PATENT EXAMINER
GROUP